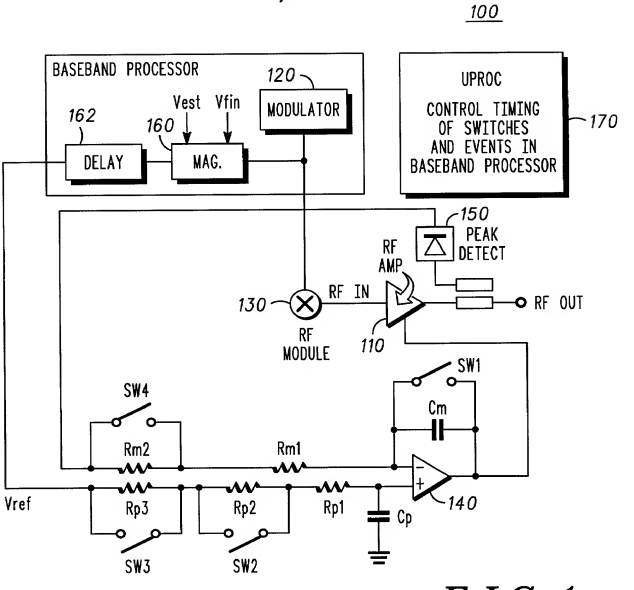

FIG.1

V_{EST1}	P_{LVL}
V_{EST1}	P_1
V_{EST2}	P_2
V_{EST3}	P_3
•	•
•	•
•	•

FIG.2

300

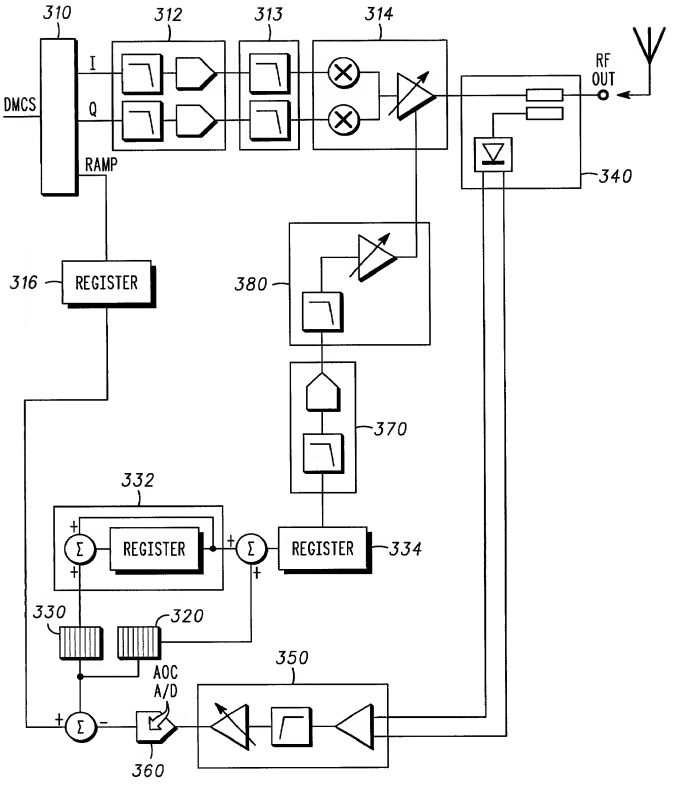
310
312
313
314
I
Q
DMCS
RAMP
RF
OUT
340
316
REGISTER
380
370
332
REGISTER
REGISTER
334
330
320
AOC
A/D
350
360

FIG. 3

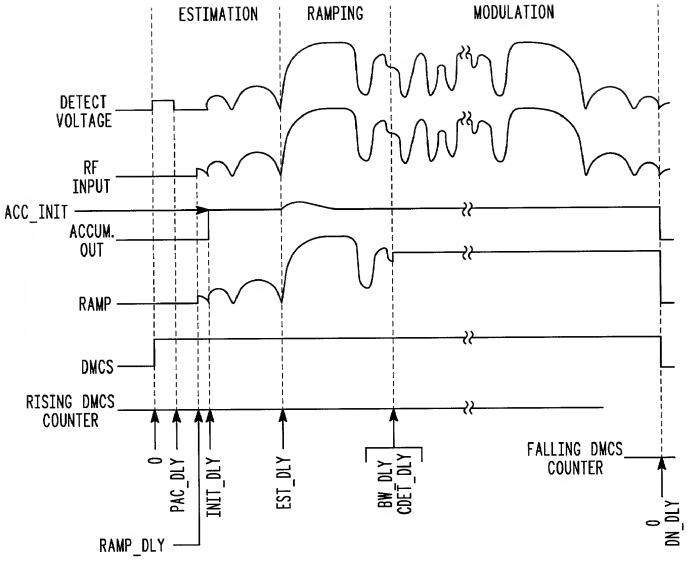
ESTIMATION
RAMPING
MODULATION
DETECT VOLTAGE
RF INPUT
ACC_INIT
ACCUM. OUT
RAMP
DMCS
RISING DMCS COUNTER
FALLING DMCS COUNTER
0
PAC_DLY
INIT_DLY
EST_DLY
BW_DLY
COEF_DLY
0
DN_DLY
RAMP_DLY

FIG. 4

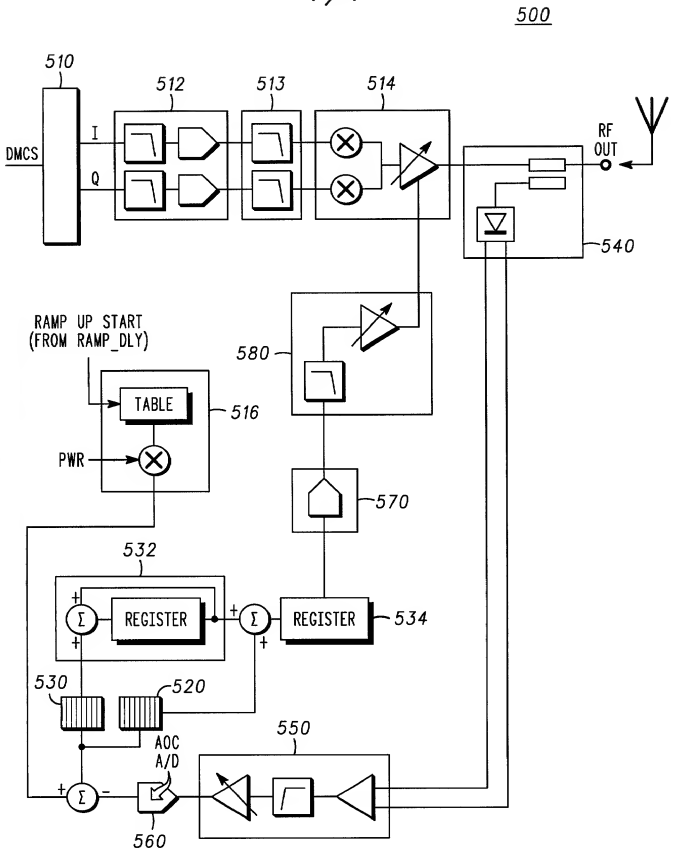
500
510
512
513
514
DMCS
I
Q
RF
OUT
540
RAMP UP START
(FROM RAMP_DLY)
580
TABLE
516
PWR
570
532
REGISTER
REGISTER
534
530
520
550
AOC
A/D
560

FIG. 5

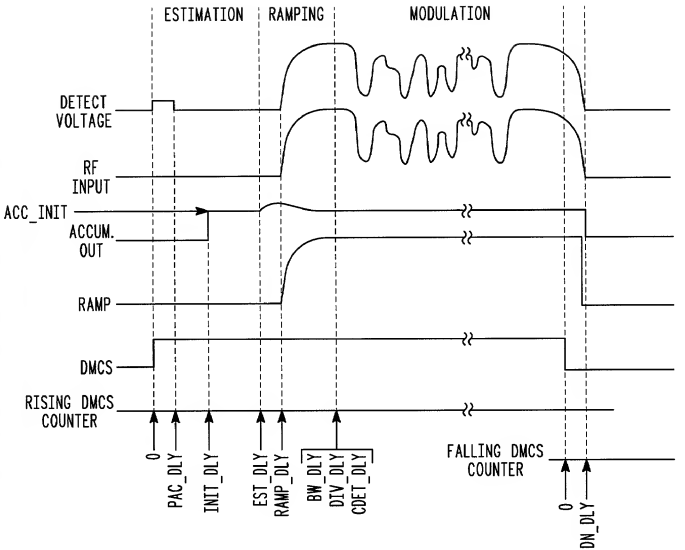
ESTIMATION
RAMPING
MODULATION
DETECT VOLTAGE
RF INPUT
ACC_INIT
ACCUM. OUT
RAMP
DMCS
RISING DMCS COUNTER
0
PAC_DLY
INIT_DLY
EST_DLY
RAMP_DLY
BW_DLY
DIV_DLY
CDET_DLY
FALLING DMCS COUNTER
0
DN_DLY

FIG.6

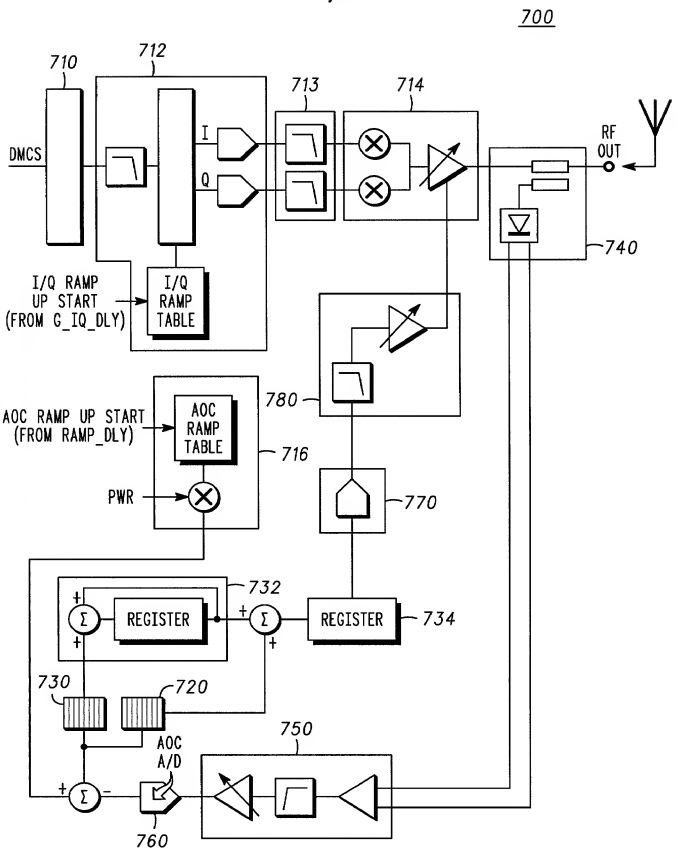
700
710
712
713
714
DMCS
I
Q
RF
OUT
740
I/Q RAMP
UP START
(FROM C_IQ_DLY)
I/Q
RAMP
TABLE
780
AOC RAMP UP START
(FROM RAMP_DLY)
AOC
RAMP
TABLE
716
PWR
770
732
REGISTER
REGISTER
734
730
720
750
AOC
A/D
760

FIG. 7

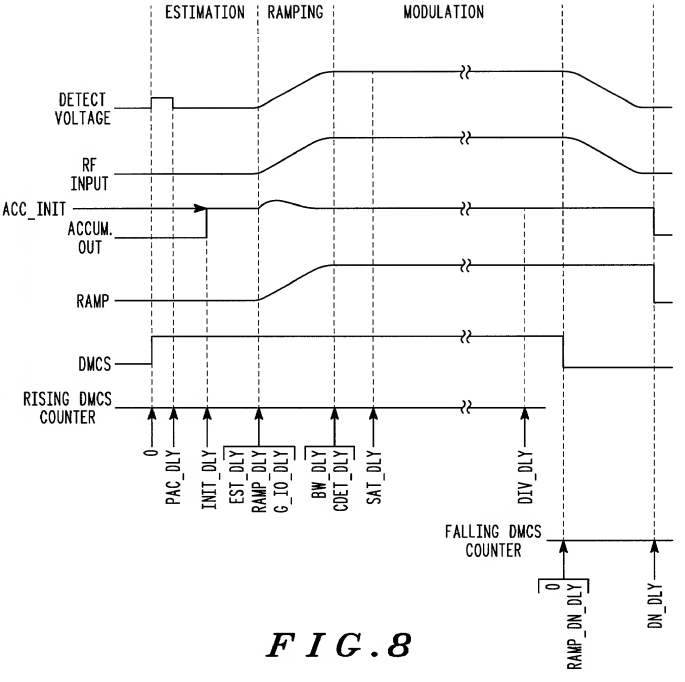
ESTIMATION
RAMPING
MODULATION
DETECT VOLTAGE
RF INPUT
ACC_INIT
ACCUM. OUT
RAMP
DMCS
RISING DMCS COUNTER
0
PAC_DLY
INIT_DLY
EST_DLY
RAMP_DLY
G_IO_DLY
BW_DLY
CDET_DLY
SAT_DLY
DIV_DLY
FALLING DMCS COUNTER
0
RAMP_DN_DLY
DN_DLY

FIG. 8